PATENT ABSTRACTS OF JAPAN

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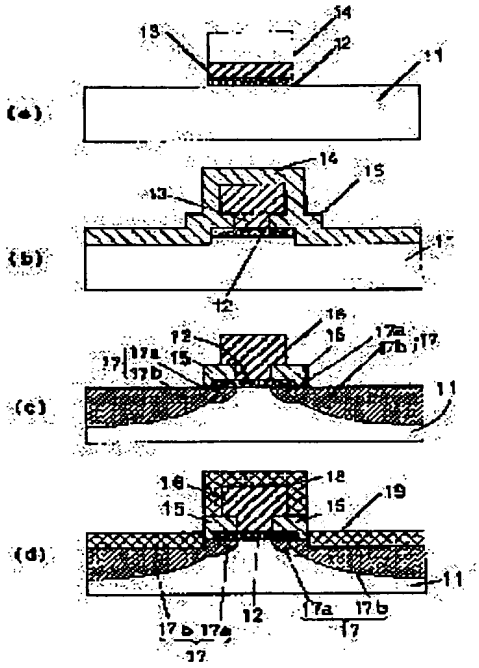
(54) MOS TYPE SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce capacitance between a gate and a drain as increasing driving force while lowering gate resistance.
SOLUTION: Doped polycrystalline silicon 13 and non-doped polycrystalline silicon 14 are deposited onto a P-type Si substrate 11 as a conductor layer for forming a gate electrode through an Si3N4 gate insulating film 12, and patterned, and the gate electrode 16 having ideal T type structure having a pair of side-wall oxide films 15 can be formed because the doped polycrystalline silicon 13 has oxidizing velocity larger than other sections when the P-type Si substrate 11, the doped polycrystalline silicon 13 and the non-doped polycrystalline silicon 14 are oxidized. Joining sections on the surface of the P-type Si substrate 11 in sections having shallow junction depth in N-type high- concentration diffusion layers 17 shaped to the P-type Si substrate by ion implantation coincide with the opposed end sections of a pair of side wall oxide films 15. Not only a metallic silicide layer 18 is formed to the upper section of the gate electrode 16 but also metallic silicide layers 19 are shaped to side sections.



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CLAIMS

[Claim(s)]
[Claim 1] The semi-conductor substrate of the 1st conductivity type, and the gate dielectric film alternatively formed in one principal plane of said semi-conductor substrate, The gate electrode prepared on said gate dielectric film, and the side-attachment-wall oxide film of the pair which was formed between the both ends of said gate electrode, and said gate dielectric film, and was prolonged to the method of outside [location / of said gate electrode / both-ends], The high concentration diffusion layer of the 2nd conductivity type of a pair with which the junction location in said semi-conductor substrate front face serves as the source/drain in accordance with the opposite edge of the side-attachment-wall oxide film of said pair while being formed in the field which sandwiches said gate dielectric film of said semi-conductor substrate and having the shallow junction depth under the side-attachment-wall oxide film of said pair, The MOS mold semiconductor device equipped with the 1st metal silicide film formed over the upper part and the flank of said gate electrode.
[Claim 2] The MOS mold semiconductor device according to claim 1 whose gate dielectric film is a nitride.
[Claim 3] The MOS mold semiconductor device according to claim 1 or 2 characterized by forming the 2nd metal silicide film in the surface section of the high concentration diffusion layer of the 2nd conductivity type of a pair.
[Claim 4] The process which forms gate dielectric film in one principal plane of the semi-conductor substrate of the 1st conductivity type, The process which deposits in order the 1st conductive film by which ion was doped, and the 2nd conductive film with which ion is not doped on said gate dielectric film, The process which carries out patterning of the photoresist to the position which becomes a gate electrode on said 2nd conductive film, The process alternatively etched until one principal plane of said semi-conductor substrate exposes the multilayers which consist of said gate dielectric film, said 1st conductive film, and said 2nd conductive film by using said photoresist as a mask by perpendicularly strong anisotropic etching, The process which forms a side-attachment-wall oxide film of a pair with which the oxide film which grows up to be the flank of said 1st conductive film according to the process which removes said photoresist, and an oxidation process becomes thicker than the oxide film which grows up to be said the 2nd flank and upper part, and said semi-conductor substrate of the conductive film, The process which makes the condition of having projected from the flank of said 2nd conductive film save the oxide film which removed the oxide film which grew up to be said the 2nd flank and upper part, and said semi-conductor substrate of the conductive film by isotropic etching, and grew up to be the flank of said 1st conductive film, While having the shallow junction depth under the side-attachment-wall oxide film of said pair with ion-implantation The process which forms the high concentration diffusion layer of the 2nd conductivity type of a pair with which the junction location in said semi-conductor substrate front face serves as the source/drain in accordance with the opposite edge of the side-attachment-wall oxide film of said pair in the field which sandwiches said gate dielectric film of said semi-conductor substrate, The process which deposits a metal membrane on said semi-conductor substrate and said gate electrode, The manufacture approach of an MOS mold semiconductor device including the process which silicide-izes said metal membrane located in the upper part of said gate electrode, and a flank and the surface section of the high concentration diffusion layer of the 2nd conductivity type of said pair, and the process which removes said metal membrane which was not silicide-ized.
[Claim 5] The manufacture approach of an MOS mold semiconductor device according to claim 4 that gate dielectric film is a nitride.
[Claim 6] The manufacture approach of the MOS mold semiconductor device a publication according to claim 4 o 5 that the 1st and 2nd conductive film is polycrystal silicone films.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention can realize super-high integration of an integrated circuit, and high-speed operation is possible for it, and it relates to the MOS mold semiconductor device and its manufacture approach of a low power.
[0002]
[Description of the Prior Art] In very-large-scale-integration equipment ******** VLSI, as for the MOS mold semiconductor device, detailed-ization of a device is performed from the request of super-high integration, high-speed operation, and low-power-izing. It is becoming impossible to already maintain the circuit property according to the trend of a scaling according to increase of the parasitic effect, i.e., parasitic capacitance, and parasitism resistance with detailed-izing of this device. Specifically, there are the following two big troubles.
[0003] 1) Among the capacity between gate drains which has big effect on a circuit property, although gate drain overlap capacity (capacity produced into the part which the gate electrode and the drain field have countered) decreases with detailed-izing, regularity and since an oxide film becomes thin rather, fringe capacity (capacity produced between the side attachment wall of a gate electrode and a drain field) increases, without carrying out a scaling. Therefore, the rate of the fringe capacity occupied in the whole capacity between gate drains increases, and the circuit property corresponding to a scaling cannot be expected.
[0004] 2) By the increment in the gate resistance of the unit gate width by reduction in gate length, if the same gate width compares, the rate of occupying to the time delay of the whole RC prolonged effect of a gate electrode with detailed-izing will increase. There are the following examples as a means to solve these two troubles. There is a salicide process as structure of there being T form gate structure as structure of reducing the capacity between gate drains of 1), and reducing the gate resistance of 2. As the typical reference, in 1, it is introduced to I.E.E.E 1991 I.E.D.M.Technical Digest pp 541-544, and is introduced to IEEE Trans.on ED, ED-29, 1982, and pp 531-535 by 2.
[0005] The example of the MOS mold semiconductor device (MOSFET) using the above T mold gate structure and salicide process is shown in drawing 3 . The P-type semiconductor substrate with which 21 consists of an Si substrate which added the P type impurity in drawing 3 , The gate oxide which formed 22 in the principal plane of the P-type semiconductor substrate 21 alternatively, The gate electrode of T form in which 23 was formed on gate oxide 22, an N type high concentration diffusion layer with shallow 24 (about [2x1019cm -] 3), 25 is SiO2. A sidewall, an N type high concentration diffusion layer with deep 26 (about [2x1020cm -] 3), The metal silicide film which formed 27 in the upper part of a gate electrode by the salicide process, and 28 are the metal silicide film formed in the surface section of an N type high concentration diffusion layer by the salicide process.
[0006]
[Problem(s) to be Solved by the Invention] However, the structure which adopted the above T mold gate structures and salicide processes is not enough as an MOS mold semiconductor device below a deep submicron field. The reason is for structure top driving force to seldom increase, even if gate length becomes small with the conventional T mold gate structure.
[0007] Drawing 4 is drawing showing the transconductance of N-channel metal oxide semiconductor FET of the conventional example, and gate length's relation, an axis of abscissa shows gate length Lgate (micrometer), and the axis of ordinate shows the transconductance Gm (mS/mm) per unit gate width. In addition, Transconductance Gm is expressed with **Ids/**Vgs, when the drain current of N-channel metal oxide semiconductor FET is set to Ids and gate voltage is set to Vgs.

[0008] In drawing 4 , the top curve is the property of N-channel metal oxide semiconductor FET of the usual structure, and reoxidation thickness supports [three lower curves] 16nm, 24nm, and 36nm respectively in the property of N-channel metal oxide semiconductor FET of T mold gate structure. The gate oxidation thickness tOX is 4nm, and this MOSFET is single drain structure. With the usual structure, if gate length becomes small, to a transconductance increasing, even if gate length becomes small, a transconductance will seldom increase, and driving force will not increase from drawing 4 by T mold gate structure.
[0009] The reason is as explaining below. That is, it is very difficult to make a long and slender BAZU beak at a gate edge, and to control the tip location correctly, therefore it difficult to double exactly the junction location of the boundary of the P-type semiconductor substrate 21 in the front face of the P-type semiconductor substrate 21 of drawing 3 , and the shallow N type high concentration diffusion field 24, i.e., the P-type semiconductor substrate 21 and the shallow N type high concentration diffusion field 24, at the edge of the leg of the gate electrode 23 of T mold. If spacing of a junction location is set up narrowly, since the shallow N type high concentration diffusion field 24 of both the source and a drain will be connected on the front face of the P-type semiconductor substrate 21 depending on the case and the channel of an MOS mold semiconductor device will be lost, the shallow N type high concentration diffusion field 24 must be formed so that a junction location may become outside [directly under / of the leg of the gate electrode 23 of T mold] approach.
[0010] However, if the field (field outside the leg of the gate electrode 23 of T mold) of an oxide film with an above-mentioned thick junction location is started The field of a before [from the edge of the leg of the gate electrode 23 of T mold in the front face of the P-type semiconductor substrate 21 / a junction location] Since the thickness of the gate oxide 22 between the gate electrodes 23 is thick, electric field cannot be added easily, moreover are not doped by N type, but since it is still P type Even if it forms the channel section directly under the leg of the gate electrode 23 of T mold by applying gate voltage to the gate electrode 23 The P type field from the channel section to that of the shallow N type high concentration diffusion layer 24 becomes very strong parasitism resistance, and even if resistance of the channel section is small, a ** rule will be carried out by the parasitism resistance, and although gate length becomes short, driving force will not increase the whole transconductance. Moreover, since the oxide film thickness of a core also becomes thick with growth of the BAZU beak by reoxidation, effectual gate oxidization thickness increases and resistance of the channel section increases. This phenomenon becomes so remarkable that gate length becomes small. The increment in driving force is restricted also at this point.
[0011] Moreover, in MOSFET whose gate oxidation thickness gate width is 4nm in 10 micrometers, if it assumes that sheet resistance is 10 ohms / ** extent, RC delay of the gate electrode will become 9ps extent. If this RC delay has fixed sheet resistance, it bases on gate length and is fixed. For example, in a 0.15-micrometer CMOS process, the gate delay is predicted to be 30ps extent, and, as for RC delay of a gate electrode, about 1/of gate length becomes whole 3 and a whole, very big thing.
[0012] The purpose of this invention is offering the MOS mold semiconductor device which can fully reduce gate resistance, and its manufacture approach while being able to reduce the capacity between gate drains, making driving force increase to below a deep submicron field.
[0013]
[Means for Solving the Problem] An MOS mold semiconductor device according to claim 1 forms gate dielectric film in one principal plane of the semi-conductor substrate of the 1st conductivity type alternatively. Prepare a gate electrode on gate dielectric film, and the side-attachment-wall oxide film of the pair prolonged to the method of outside [location / of a gate electrode / both-ends] is formed between the both ends of a gate electrode, and gate dielectric film. The high concentration diffusion layer of the 2nd conductivity type of a pair with which the junction location in a semi-conductor substrate front face serves as the source/drain in accordance with the opposite edge of the side-attachment-wall oxide film of a pair while having the shallow junction depth under the side-attachment-wall oxide film of a pair to the field which sandwiches the gate dielectric film of a semi-conductor substrate is formed. The 1st metal silicide film is formed over the upper part and the flank of a gate electrode.
[0014] According to this MOS mold semiconductor device, the side-attachment-wall oxide film of the pair prolonged to the method of outside [location / of a gate electrode / both-ends] is formed between the both ends of a gate electrode, and gate dielectric film, a gate electrode serves as T mold gate structure, and the distance between the high concentration diffusion layers of the 2nd conductivity type of the pair which is the flank, and a drain/source of a gate electrode increases, therefore the capacity between gate drains is reduced. Moreover, since gate voltage be effectively apply to the whole field of the semi-conductor substrate which serve

as the channel section under gate dielectric film since the junction location in the semi-conductor substrate front face of the high concentration diffusion layer of the 2nd conductivity type of a pair be in agreement with the opposite edge of the side attachment wall oxide film of a pair and the part of high resistance do not remain in the bottom of the side attachment wall oxide film of a pair, driving force will increase only the part to which gate length became short in connection with T mold gate structure. Moreover, since the 1st metal silicide film is formed not only in the upper part of a gate electrode but in a flank, gate resistance is fully reduced. Moreover, since it has the junction depth with the 2nd high concentration diffusion layer shallow under the side-attachment-wall oxide film of a pair, it becomes a device very strong against the short channel effect.

[0015] The MOS mold semiconductor device according to claim 2 makes gate dielectric film the nitride in the MOS mold semiconductor device according to claim 1.

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TECHNICAL FIELD

[Field of the Invention] This invention can realize super-high integration of an integrated circuit, and high-speed operation is possible for it, and it relates to the MOS mold semiconductor device and its manufacture approach of a low power.

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PRIOR ART

[Description of the Prior Art] In very-large-scale-integration equipment ******** VLSI, as for the MOS mold semiconductor device, detailed-ization of a device is performed from the request of super-high integration, high-speed operation, and low-power-izing. It is becoming impossible to already maintain the circuit property according to the trend of a scaling according to increase of the parasitic effect, i.e., parasitic capacitance, and parasitism resistance with detailed-izing of this device. Specifically, there are the following two big troubles.
[0003] 1) Among the capacity between gate drains which has big effect on a circuit property, although gate drain overlap capacity (capacity produced into the part which the gate electrode and the drain field have countered) decreases with detailed-izing, regularity and since an oxide film becomes thin rather, fringe capacity (capacity produced between the side attachment wall of a gate electrode and a drain field) increases, without carrying out a scaling. Therefore, the rate of the fringe capacity occupied in the whole capacity between gate drains increases, and the circuit property corresponding to a scaling cannot be expected.
[0004] 2) By the increment in the gate resistance of the unit gate width by reduction in gate length, if the same gate width compares, the rate of occupying to the time delay of the whole RC prolonged effect of a gate electrode with detailed-izing will increase. There are the following examples as a means to solve these two troubles. There is a salicide process as structure of there being T form gate structure as structure of reducing the capacity between gate drains of 1), and reducing the gate resistance of 2. As the typical reference, in 1, it is introduced to I.E.E.E 1991 I.E.D.M.Technical Digest pp 541-544, and is introduced to IEEE Trans.on ED, ED-29, 1982, and pp 531-535 by 2.
[0005] The example of the MOS mold semiconductor device (MOSFET) using the above T mold gate structure and salicide process is shown in drawing 3 . The P-type semiconductor substrate with which 21 consists of an Si substrate which added the P type impurity in drawing 3 , The gate oxide which formed 22 in the principal plane of the P-type semiconductor substrate 21 alternatively, The gate electrode of T form in which 23 was formed on gate oxide 22, an N type high concentration diffusion layer with shallow 24 (about [2x1019cm -] 3), 25 is SiO2. A sidewall, an N type high concentration diffusion layer with deep 26 (about [2x1020cm -] 3), The metal silicide film which formed 27 in the upper part of a gate electrode by the salicide process, and 28 are the metal silicide film formed in the surface section of an N type high concentration diffusion layer by the salicide process.

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EFFECT OF THE INVENTION

[Effect of the Invention] Since the side-attachment-wall oxide film of the pair prolonged to the method of outside [location / of a gate electrode / both-ends] was formed between the both ends of a gate electrode, and gate dielectric film according to the MOS mold semiconductor device according to claim 1, it can become T mold gate structure, and the distance between the flank of a gate electrode and a drain can be earned, therefore the capacity between gate drains can be reduced. Moreover, since gate voltage can be effectively applied to the whole field of the semi-conductor substrate which serve as the channel section under gate dielectric film since the junction location in the semi-conductor substrate front face of the high concentration diffusion layer of the 2nd conductivity type of a pair be made in agreement with the opposite edge of the side attachment wall oxide film of a pair and the part of high resistance do not remain in the bottom of the side attachment wall oxide film of a pair, in connection with T mold gate structure, only the part to which gate length became short can increase driving force. Moreover, since the 1st metal silicide film is formed not only in the upper part of a gate electrode but in a flank, gate resistance can fully be reduced. Moreover, since it has the junction depth with the 2nd high concentration diffusion layer shallow under the side-attachment-wall oxide film of a pair, it becomes a device very strong against the short channel effect.
[0034] According to the MOS mold semiconductor device according to claim 2, supply of the oxygen from gate dielectric film to the gate electrode on it is intercepted. Since oxygen becomes [being supplied from the side attachment wall of a gate electrode, and] and oxygen is not supplied to the core of a gate electrode in case the side-attachment-wall oxide film of a pair is formed on gate dielectric film An oxide film will run from the side attachment wall of a gate electrode to gate dielectric film and abbreviation parallel toward the interior of a gate electrode, it is stopped that the side-attachment-wall oxide film of a pair becomes BAZU beak-like, it will be in the condition near an abbreviation square, and a gate electrode can be brought close to ideal T mold. Therefore, it becomes easy to lengthen the leg of T mold, without making the leg of T mold thin, and it becomes possible to reduce the capacity between gate drains further.
[0035] According to the MOS mold semiconductor device according to claim 3, resistance of the source/drain can also be decreased. According to the manufacture approach of an MOS mold semiconductor device according to claim 4, the gate electrode has two-layer structure of the 1st conductive film by which ion was doped, and the 2nd conductive film with which ion is not doped, and at an oxidation process, since the oxidation rate of the 1st conductive film is larger than the oxidation rate of the non dope polycrystalline silicon which is the 2nd conductive film, the configuration of a gate electrode can be used as T mold. Therefore, capacity between gate drains can be made small.
[0036] Moreover, since gate voltage can be effectively apply to the whole field of the semi-conductor substrate which serve as the channel section under gate dielectric film since the junction location in a semi-conductor substrate front face be make in agreement with the opposite edge of the side attachment wall oxide film of a pair gate voltage be effectively apply to the bottom of the side attachment wall oxide film of a pair and the part of high resistance do not remain, in connection with T mold gate structure, only the part to which gate length became short can increase driving force. In addition, it is because the junction location of the high concentration diffusion layer which can control the die length with a sufficient precision, therefore is formed by the ion implantation since the side-attachment-wall oxide film of a pair is formed using the difference in an oxidation rate can be easily doubled with the opposite edge of the side-attachment-wall oxide film of a pair that driving force can be made to increase easily.
[0037] Moreover, with the side-attachment-wall oxide film of a pair, since the silicide layer on a gate electrode and the silicide layer of the source/drain can be insulated,-izing not only of the upper part of a gate electrode

but the flank can be carried out [silicide], and it can fully reduce gate resistance. Moreover, a high concentration diffusion layer with the shallow junction depth and a high concentration diffusion layer with the deep junction depth, i.e., the extension source / drain, can be formed at 1 time of an impregnation process with the side-attachment-wall oxide film of a pair.

[0038] According to the manufacture approach of an MOS mold semiconductor device according to claim 5, supply of the oxygen from gate dielectric film to the gate electrode on it is intercepted. Since oxygen becomes [being supplied from the side attachment wall of a gate electrode, and] and oxygen is not supplied to the core of a gate electrode in case the side-attachment-wall oxide film of a pair is formed on gate dielectric film An oxide film will run from the side attachment wall of a gate electrode to gate dielectric film and abbreviation parallel toward the interior of a gate electrode, it is stopped that the side-attachment-wall oxide film of a pair becomes BAZU beak-like, it will be in the condition near an abbreviation square, and a gate electrode can be brought close to ideal T mold. Therefore, it becomes easy to lengthen the leg of T mold, without making the leg of T mold thin, and it becomes possible to reduce the capacity between gate drains further.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the structure which adopted the above T mold gate structures and salicide processes is not enough as an MOS mold semiconductor device below a deep submicron field. The reason is for structure top driving force to seldom increase, even if gate length becomes small with the conventional T mold gate structure.
[0007] Drawing 4 is drawing showing the transconductance of N-channel metal oxide semiconductor FET of the conventional example, and gate length's relation, an axis of abscissa shows gate length Lgate (micrometer), and the axis of ordinate shows the transconductance Gm (mS/mm) per unit gate width. In addition, Transconductance Gm is expressed with **Ids/**Vgs, when the drain current of N-channel metal oxide semiconductor FET is set to Ids and gate voltage is set to Vgs.
[0008] In drawing 4 , the top curve is the property of N-channel metal oxide semiconductor FET of the usual structure, and reoxidation thickness supports [three lower curves] 16nm, 24nm, and 36nm respectively in the property of N-channel metal oxide semiconductor FET of T mold gate structure. The gate oxidation thickness tOX is 4nm, and this MOSFET is single drain structure. With the usual structure, if gate length becomes small, to a transconductance increasing, even if gate length becomes small, a transconductance will seldom increase, and driving force will not increase from drawing 4 by T mold gate structure.
[0009] The reason is as explaining below. That is, it is very difficult to make a long and slender BAZU beak at a gate edge, and to control the tip location correctly, therefore it difficult to double exactly the junction location of the boundary of the P-type semiconductor substrate 21 in the front face of the P-type semiconductor substrate 21 of drawing 3 , and the shallow N type high concentration diffusion field 24, i.e., the P-type semiconductor substrate 21 and the shallow N type high concentration diffusion field 24, at the edge of the leg of the gate electrode 23 of T mold. If spacing of a junction location is set up narrowly, since the shallow N type high concentration diffusion field 24 of both the source and a drain will be connected on the front face of the P-type semiconductor substrate 21 depending on the case and the channel of an MOS mold semiconductor device will be lost, the shallow N type high concentration diffusion field 24 must be formed so that a junction location may become outside [directly under / of the leg of the gate electrode 23 of T mold] approach.
[0010] However, if the field (field outside the leg of the gate electrode 23 of T mold) of an oxide film with an above-mentioned thick junction location is started The field of a before [from the edge of the leg of the gate electrode 23 of T mold in the front face of the P-type semiconductor substrate 21 / a junction location] Since the thickness of the gate oxide 22 between the gate electrodes 23 is thick, electric field cannot be added easily, moreover are not doped by N type, but since it is still P type Even if it forms the channel section directly under the leg of the gate electrode 23 of T mold by applying gate voltage to the gate electrode 23 The P type field from the channel section to that of the shallow N type high concentration diffusion layer 24 becomes very strong parasitism resistance, and even if resistance of the channel section is small, a ** rule will be carried out by the parasitism resistance, and although gate length becomes short, driving force will not increase the whole transconductance. Moreover, since the oxide film thickness of a core also becomes thick with growth of the BAZU beak by reoxidation, effectual gate oxidization thickness increases and resistance of the channel section increases. This phenomenon becomes so remarkable that gate length becomes small. The increment in driving force is restricted also at this point.
[0011] Moreover, in MOSFET whose gate oxidation thickness gate width is 4nm in 10 micrometers, if it assumes that sheet resistance is 10 ohms / ** extent, RC delay of the gate electrode will become 9ps extent. If this RC delay has fixed sheet resistance, it bases on gate length and is fixed. For example, in a 0.15-micrometer CMOS process, the gate delay is predicted to be 30ps extent, and, as for RC delay of a gate electrode, about 1/of gate

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[0011] Moreover, in MOSFET whose gate oxidation thickness gate width is 4nm in 10 micrometers, if it assumes that sheet resistance is 10 ohms / ** extent, RC delay of the gate electrode will become 9ps extent. If this RC delay has fixed sheet resistance, it bases on gate length and is fixed. For example, in a 0.15-micrometer CMOS process, the gate delay is predicted to be 30ps extent, and, as for RC delay of a gate electrode, about 1/of gate

length becomes whole 3 and a whole, very big thing.
[0012] The purpose of this invention is offering the MOS mold semiconductor device which can fully reduce gate resistance, and its manufacture approach while being able to reduce the capacity between gate drains, making driving force increase to below a deep submicron field.

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MEANS

[Means for Solving the Problem] An MOS mold semiconductor device according to claim 1 forms gate dielectric film in one principal plane of the semi-conductor substrate of the 1st conductivity type alternatively. Prepare a gate electrode on gate dielectric film, and the side-attachment-wall oxide film of the pair prolonged to the method of outside [location / of a gate electrode / both-ends] is formed between the both ends of a gate electrode, and gate dielectric film. The high concentration diffusion layer of the 2nd conductivity type of a pair with which the junction location in a semi-conductor substrate front face serves as the source/drain in accordance with the opposite edge of the side-attachment-wall oxide film of a pair while having the shallow junction depth under the side-attachment-wall oxide film of a pair to the field which sandwiches the gate dielectric film of a semi-conductor substrate is formed. The 1st metal silicide film is formed over the upper part and the flank of a gate electrode.
[0014] According to this MOS mold semiconductor device, the side-attachment-wall oxide film of the pair prolonged to the method of outside [location / of a gate electrode / both-ends] is formed between the both ends of a gate electrode, and gate dielectric film, a gate electrode serves as T mold gate structure, and the distance between the high concentration diffusion layers of the 2nd conductivity type of the pair which is the flank, and a drain/source of a gate electrode increases, therefore the capacity between gate drains is reduced. Moreover, since gate voltage be effectively apply to the whole field of the semi-conductor substrate which serve as the channel section under gate dielectric film since the junction location in the semi-conductor substrate front face of the high concentration diffusion layer of the 2nd conductivity type of a pair be in agreement with the opposite edge of the side attachment wall oxide film of a pair and the part of high resistance do not remain in the bottom of the side attachment wall oxide film of a pair, driving force will increase only the part to which gate length became short in connection with T mold gate structure. Moreover, since the 1st metal silicide film is formed not only in the upper part of a gate electrode but in a flank, gate resistance is fully reduced. Moreover, since it has the junction depth with the 2nd high concentration diffusion layer shallow under the side-attachment-wall oxide film of a pair, it becomes a device very strong against the short channel effect.
[0015] The MOS mold semiconductor device according to claim 2 makes gate dielectric film the nitride in the MOS mold semiconductor device according to claim 1. According to this MOS mold semiconductor device, supply of the oxygen from gate dielectric film to the gate electrode on it is intercepted. Since oxygen becomes [being supplied from the side attachment wall of a gate electrode, and] and oxygen is not supplied to the core of a gate electrode in case the side-attachment-wall oxide film of a pair is formed on gate dielectric film An oxide film will run from the side attachment wall of a gate electrode to gate dielectric film and abbreviation parallel toward the interior of a gate electrode, it is stopped that the side-attachment-wall oxide film of a pair becomes BAZU beak-like, it will be in the condition near an abbreviation square, and a gate electrode will be in the condition near ideal T mold. Therefore, it becomes easy to lengthen the leg of T mold, without making the leg of T mold thin, and the capacity between gate drains is reduced further.
[0016] The MOS mold semiconductor device according to claim 3 forms the 2nd metal silicide film in the surface section of the high concentration diffusion layer of the 2nd conductivity type of a pair in an MOS mold semiconductor device according to claim 1 or 2. According to this MOS mold semiconductor device, resistance of the source/drain will also decrease. The manufacture approach of an MOS mold semiconductor device according to claim 4 Form gate dielectric film in one principal plane of the semi-conductor substrate of the 1st conductivity type, and the 1st conductive film by which ion was doped on this gate dielectric film, and the 2nd conductive film with which ion is not doped are deposited in order. Subsequently, patterning of the photoresist is carried out to the position which becomes a gate electrode on the 2nd conductive film. It etches alternatively until one principal

plane of a semi-conductor substrate exposes the multilayers which consist of gate dielectric film, the 1st conductive film, and the 2nd conductive film by using a photoresist as a mask by perpendicularly strong anisotropic etching. Then, remove a photoresist and a side-attachment-wall oxide film of a pair with which the oxide film which grows up to be the flank of the 1st conductive film according to an oxidation process becomes thicker than the oxide film which grows up to be the 2nd flank and upper part, and semi-conductor substrate of the conductive film is formed. Subsequently, the oxide film which grew up to be the 2nd flank and upper part, and semi-conductor substrate of the conductive film by isotropic etching is removed, and the condition of having projected from the flank of the 2nd conductive film is made to save the oxide film which grew up to be the flank of the 1st conductive film. Next The high concentration diffusion layer of the 2nd conductivity type of a pair with which the junction location in a semi-conductor substrate front face serves as the source/drain in accordance with the opposite edge of the side-attachment-wall oxide film of said pair while having the shallow junction depth under the side-attachment-wall oxide film of a pair with ion-implantation is formed in the field which sandwiches the gate dielectric film of a semi-conductor substrate. The metal membrane which deposited the metal membrane on the semi-conductor substrate and the gate electrode, silicide-ized the metal membrane subsequently to the upper part of a gate electrode, and a flank and the surface section of the high concentration diffusion layer of the 2nd conductivity type of a pair located, and was not silicide-ized after that is removed.

[0017] According to the manufacture approach of this MOS mold semiconductor device, the gate electrode has two-layer structure of the 1st conductive film (for example, it consists of dope polycrystalline silicon) by which ion was doped, and the 2nd conductive film (for example, it consists of non dope polycrystalline silicon) with which ion is not doped. At an oxidation process, since the oxidation rate of the 1st conductive film is larger than the oxidation rate of the 2nd conductive film, the configuration of a gate electrode becomes T mold. Therefore, the capacity between gate drains becomes small.

[0018] moreover , since gate voltage can be effectively apply to the whole field of the semi-conductor substrate which serve as the channel section under gate dielectric film since the junction location in a semi-conductor substrate front face be make in agreement with the opposite edge of the side attachment wall oxide film of a pair and the part of high resistance do not remain in the bottom of the side attachment wall oxide film of a pair , it come to be alike that driving force increase only the part to which gate length became short in connection with T mold gate structure In addition, it is because the junction location of the high concentration diffusion layer which can control the die length with a sufficient precision, therefore is formed by the ion implantation since the side-attachment-wall oxide film of a pair is formed using the difference in an oxidation rate can be easily doubled with the opposite edge of the side-attachment-wall oxide film of a pair that it is possible to make driving force increase.

[0019] Moreover, with the side-attachment-wall oxide film of a pair, since the silicide layer on a gate electrode and the silicide layer of the source/drain are insulated,-izing not only of the upper part of a gate electrode but the flank can be carried out [silicide], and gate resistance is fully reduced. Moreover, a high concentration diffusion layer with the shallow junction depth and a high concentration diffusion layer with the deep junction depth, i.e., the extension source / drain, are formed at 1 time of an impregnation process with the side-attachment-wall oxide film of a pair.

[0020] The manufacture approach of an MOS mold semiconductor device according to claim 5 makes gate dielectric film the nitride in the manufacture approach of an MOS mold semiconductor device according to claim 4. According to this MOS mold semiconductor device, supply of the oxygen from gate dielectric film to the gate electrode on it is intercepted, in case the side-attachment-wall oxide film of a pair is formed on gate dielectric film, oxygen becomes [being supplied from the side attachment wall of a gate electrode, and], and oxygen is not supplied to the core of a gate electrode. Therefore, an oxide film will run from the side attachment wall of a gate electrode to gate dielectric film and abbreviation parallel toward the interior of a gate electrode, it is stopped that the side-attachment-wall oxide film of a pair becomes BAZU beak-like, it will be in the condition near an abbreviation square, and a gate electrode will be in the condition near ideal T mold. Therefore, it becomes easy to lengthen the leg of T mold, without making the leg of T mold thin, and the capacity between gate drains is reduced further.

[0021] The manufacture approach of an MOS mold semiconductor device according to claim 6 is using the 1st and 2nd conductive film as the polycrystal silicone film in the manufacture approach of an MOS mold semiconductor device according to claim 4 or 5.

[0022]

[Embodiment of the Invention] Hereafter, the gestalt of operation of the MOS mold semiconductor device of this

invention and its manufacture approach is explained, referring to a drawing.
[Gestalt of operation of an MOS mold semiconductor device] Drawing 1 is a sectional view in the gestalt of operation of the MOS mold semiconductor device of this invention. In drawing 1 , 1 is a P-type semiconductor substrate which consists of an Si substrate with which the P type impurity was introduced. 2 is Si3 N4 alternatively formed on the 1 principal plane of the P-type semiconductor substrate 1. It is gate dielectric film which consists of film. 4 is the gate electrode of T mold structure established on gate dielectric film 2, and the both ends are retreating from the edge of gate dielectric film 2 to the method of inside. 3 is the side-attachment-wall oxide film of the pair formed between the edge of the gate electrode 4, and gate dielectric film 2, and the edge crossed the edge of the gate electrode 4, and has extended to the method of outside across the edge of gate dielectric film 2 further. 5 is the high concentration diffusion layer of the 2nd conductivity type of a pair with which the junction location in the front face of the P-type semiconductor substrate 1 serves as the source/drain in accordance with the opposite edge of the side-attachment-wall oxide film 3 of a pair while it is formed in the field which sandwiches the gate dielectric film 2 of the P-type semiconductor substrate 1 and has the shallow junction depth under the side-attachment-wall oxide film 3 of a pair. 5a is a shallow N type high concentration diffusion layer, and 5b is a deep N type diffusion layer. 6 is the metal silicide film formed over the upper part and the flank (except for the flank of the leg) of the gate electrode 4 of T mold structure, 7 is the metal silicide film formed in the surface section of the high concentration diffusion layer 5 of the 2nd conductivity type of a pair, this is formed of a salicide process and insulating separation is carried out with the side-attachment-wall oxide film 3 of a pair.
[0023] A characteristic thing with the structure of the MOS mold semiconductor device of drawing 1 Since the side-attachment-wall oxide film 3 of the pair which carried out the configuration of an abbreviation rectangle is in the edge of the gate electrode 4 It is the gate electrode 4 of ideal T mold structure, and the junction location of the high concentration diffusion layer 5 is doubled with the opposite edge of the side-attachment-wall oxide film 3 of this pair, It is forming the metal silicide film 6 not only in the upper part of the gate electrode 4 but in a flank, and that the junction depth of the high concentration diffusion layer 5 under the side-attachment-wall oxide film 3 of a pair is shallow.
[0024] In addition, with the gestalt of the above-mentioned implementation, although gate dielectric film 2 was constituted from a silicon nitride, it may consist of silicon oxide. Since the side-attachment-wall oxide film 3 of the pair prolonged to the method of outside [location / of the gate electrode 4 / both-ends] was formed between the both ends of the gate electrode 4, and gate dielectric film 2 according to the gestalt of this operation, it can become T mold gate structure, and the distance between the flank of the gate electrode 4 and a drain can be earned, therefore the capacity between gate drains can be reduced. Moreover, since the junction location in the front face of the P-type semiconductor substrate 1 of the high concentration diffusion layer 5 of the 2nd conductivity type of a pair was made in agreement with the opposite edge of the side-attachment-wall oxide film 3 of a pair Since gate voltage can be effectively applied to the whole field of the P-type semiconductor substrate 1 used as the channel section under gate dielectric film 2, gate voltage is not effectively applied to the bottom of the side-attachment-wall oxide film 3 of a pair and the part of high resistance does not remain In connection with T mold gate structure, only the part to which gate length became short can increase driving force. Moreover, since the 1st metal silicide film 6 is formed not only in the upper part of the gate electrode 4 but in a flank, gate resistance can fully be reduced. Moreover, since it has the junction depth with the 2nd high concentration diffusion layer 5 shallow under the side-attachment-wall oxide film 3 of a pair, it becomes a device very strong against the short channel effect.
[0025] Moreover, supply of the oxygen from gate dielectric film 2 to the gate electrode 4 on it is intercepted. Since oxygen becomes [being supplied from the side attachment wall of the gate electrode 4, and] and oxygen is not supplied to the core of the gate electrode 4 in case the side-attachment-wall oxide film 3 of a pair is formed on gate dielectric film 2 An oxide film will run from the side attachment wall of the gate electrode 4 to gate dielectric film 2 and abbreviation parallel toward the interior of the gate electrode 4, it is stopped that the side-attachment-wall oxide film 3 of a pair becomes BAZU beak-like, it will be in the condition near an abbreviation square, and the gate electrode 4 can be brought close to ideal T mold. Therefore, it becomes easy to lengthen the leg of T mold, without making the leg of T mold thin, and it becomes possible to reduce the capacity between gate drains further. Moreover, since the metal silicide film 7 is formed in the surface section of the high concentration diffusion layer 5 of the 2nd conductivity type of a pair, resistance of the source/drain can also be decreased.
[0026] [Gestalt of implementation of the manufacture approach of an MOS mold semiconductor device] Drawing

2 (a) - (d) is a process sectional view in the gestalt of implementation of the manufacture approach of the MOS mold semiconductor device of this invention. Hereafter, the manufacture approach of an MOS mold semiconductor device is explained, referring to drawing 2 . It is Si3 N4 on the P-type semiconductor substrate 11 which becomes the beginning from a P type Si substrate as first shown in drawing 2 (a). Gate dielectric film 12 is formed in about 8nm. In addition, the P-type semiconductor substrate 11 top and Si3 N4 The about 1-2nm natural oxidation film may be respectively formed in gate dielectric film 12. In that case, Si3 N4 Gate dielectric film 12 is formed in about 4nm, and it is set up so that it may be set to about 4-5nm by oxide-film conversion. In addition, as sequence of the process in this case, it is Siafter about 1-2nm natural oxidation film was formed on P-type semiconductor substrate 113 N4. Gate dielectric film 12 is deposited and it is Si3 N4 after that further. The about 1-2nm natural oxidation film will be formed on gate dielectric film 12.

[0027] Next, it is Si3 N4. On gate dielectric film 12, it deposits at 60nm of thickness, and the dope polycrystal silicone film 13 and the undoping polycrystal silicone film 14 are respectively deposited on about 140nm in order. At this time, the dope polycrystal silicone film 13 is N type, and is doped by about [2x1020cm -] three. Furthermore, patterning is carried out so that it may leave a photoresist to the position which deposits a photoresist (not shown) on the undoping polycrystal silicone film 14, and becomes the gate electrode 16 (refer to drawing 2 (c) and (d)) on the undoping polycrystal silicone film 14 after that. And it leaves the part which serves as the gate electrode 16 alternatively by performing anisotropic etching perpendicularly strong as a mask in a photoresist. Finally, a photoresist is removed.

[0028] Next, as shown in drawing 2 (b), 850-degree-C heat treatment for 15 minutes is performed in a wet oxygen ambient atmosphere (H2 O+O2 ambient atmosphere). thereby -- a total of 40nm of each and the 80nm side-attachment-wall oxide film 15 is formed [the upper part and the flank on the undoping polycrystal silicone film 14 / an outside and the inside / the flank of 20nm and the dope polycrystal silicone film 13] from the edge of the gate electrode 16 at a gate edge to an outside, and the inside on 10nm of each, a total of 20nm, and the P-type semiconductor substrate 11. In addition, the dope polycrystalline silicon 13 and the non dope polycrystal 14 which the impurity diffused become the thing of one by the above-mentioned heat treatment.

[0029] Next, as shown in drawing 2 (c), the wet etching (isotropic etching) of the conditions for NH4 F:HF=20:1, 20 degrees C, and 20 seconds removes the side-attachment-wall oxide film 15 formed on the upper part on the undoping polycrystal silicone film 14 and the flank, and the P-type semiconductor substrate 11. At this time, as for the side-attachment-wall oxide film of the flank of the dope polycrystal silicone film 13, 30nm and height are respectively set to 40nm from the edge of the gate electrode 16 at an outside and the inside. Isotropic dry etching is also possible for the above-mentioned process.

[0030] The N type high concentration diffusion layer 17 which are with the impurity of N type, impregnation energy 20keV, and an impregnation dose of about 4x1015 conditions, for example, serves as the source/drain by performing the ion implantation of As ion next gate electrode [of N type] 16 and P-type semiconductor substrate top 11 is formed. Furthermore, activation of the source / drain, and the gate electrode 16 is performed to coincidence by performing lamp annealing (RTA; rapid thermal annealing) on condition that 1000 degrees C and 10sec. At this time, the junction depth of the N type high concentration diffusion layer 17 with the junction depth of shallow N channel high concentration diffusion layer 17a under the side-attachment-wall oxide film 15 of the pair of the N type high concentration diffusion layer 17 deep [about 50nm, and the other other source/drain] is set to about 100nm. Moreover, the junction location of the N type high concentration diffusion layer 17 and location of the opposite edge of the side-attachment-wall oxide film 15 of a pair of overlap length of the source/drain which are set to about 30nm and serve as the source/drain correspond. In addition, in order to make the junction location of the N type high concentration diffusion layer 17, and the location of the opposite edge of the side-attachment-wall oxide film 15 of a pair mostly in agreement in this way, it is necessary to set up the conditions of lamp annealing, and the conditions of an ion implantation proper.

[0031] Next, Co is deposited on about 10nm and about 20nm of TiN(s) is made to deposit in order as a metal membrane, as shown in drawing 2 (d) (it is considering as two-layer structure for antioxidizing of Co). The high concentration diffusion layer 17 which serves as the source/drain of gate electrode 16 and P-type semiconductor substrate top 11 by performing 450 degrees C of 1st heat treatment for 30 minutes is silicide-ized (salicide process). Furthermore, the metal silicide film 18 and 19 is formed by etching the Co/TiN layer which was not silicide-ized on condition that NH4 OH+H2 O2+H2 O (65 degrees C, 90 seconds) and HCl+H 2O2 (a room temperature, 3 minutes). Furthermore, in order to attain low resistance-ization of the metal silicide film 18 and 19, 2nd heat treatment is performed by 750 degrees C and RTA for 30 seconds.

[0032] With the gestalt of implementation of the manufacture approach of the MOS mold semiconductor device

constituted as mentioned above, the gate electrode 16 has two-layer structure of the dope polycrystal silicone film 13 and the undoping polycrystal silicone film 14, and in an oxidation process, since the oxidation rate of the dope polycrystal silicone film 13 is large, the configuration of the gate electrode 16 can be used as T mold. Under the present circumstances, since the side-attachment-wall oxide film 15 of a pair is formed using the difference in an oxidation rate, the junction location of the high concentration diffusion layer 17 which can control that die length with a sufficient precision, therefore is formed by the ion implantation can be easily doubled with the opposite edge of the side-attachment-wall oxide film 15 of a pair, therefore driving force can be made to increase easily. Moreover, since oxygen is not supplied to the core of the gate electrode 16 since the silicon nitride film is used as gate dielectric film 12, and a BAZU beak is not formed in the edge of the gate electrode 16, the gate electrode 16 of ideal T mold structure can be made. Moreover, since the metal silicide film 19 on the high concentration diffusion layer 17 which serves as the metal silicide film 18 on the gate electrode 4, and the source/drain with the side-attachment-wall oxide film 15 of a pair can be insulated,-izing not only of the upper part of the gate electrode 16 but the flank can be carried out [silicide]. Moreover, high concentration diffusion layer 17a with the shallow junction depth and high concentration diffusion layer 17b with the deep junction depth, i.e., the extension source / drain, can be formed at 1 time of an impregnation process by existence of the side-attachment-wall oxide film 15 of a pair.

[Translation done.]

* NOTICES *

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3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the structure section Fig. showing the gestalt of operation of the MOS mold semiconductor device of this invention.
[Drawing 2] It is the structure section Fig. showing the gestalt of implementation of the manufacture approach of the MOS mold semiconductor device of this invention.
[Drawing 3] It is the structure section Fig. showing the MOS mold semiconductor device of the conventional example.
[Drawing 4] It is drawing showing the transconductance of the MOS mold semiconductor device of the conventional example, and gate length's relation.
[Description of Notations]
1 P-type Semiconductor Substrate
2 Si3 N4 Gate Dielectric Film
3 Side-Attachment-Wall Oxide Film
4 Gate Electrode
5 N Type High Concentration Diffusion Layer
5a A shallow N type high concentration diffusion layer
5b A deep N type high concentration diffusion layer
6 Metal Silicide Film
7 Metal Silicide Film
11 P-type Semiconductor Substrate
12 Si3 N4 Gate Dielectric Film
13 Dope Polycrystalline Silicon
14 Non Dope Polycrystalline Silicon
15 Side-Attachment-Wall Oxide Film
16 Gate Electrode
17 N Type High Concentration Diffusion Layer
17a A shallow N type high concentration diffusion layer
17b A deep N type high concentration diffusion layer
18 Metal Silicide Film
19 Metal Silicide Film
21 P-type Semiconductor Substrate
22 Gate Oxide
23 Gate Electrode
24 Shallow N Type High Concentration Diffusion Layer
25 SiO2 Sidewall
26 Deep N Type High Concentration Diffusion Layer
27 Metal Silicide Film
28 Metal Silicide Film

[Translation done.]

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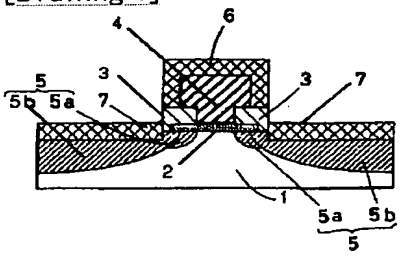
3.In the drawings, any words are not translated.

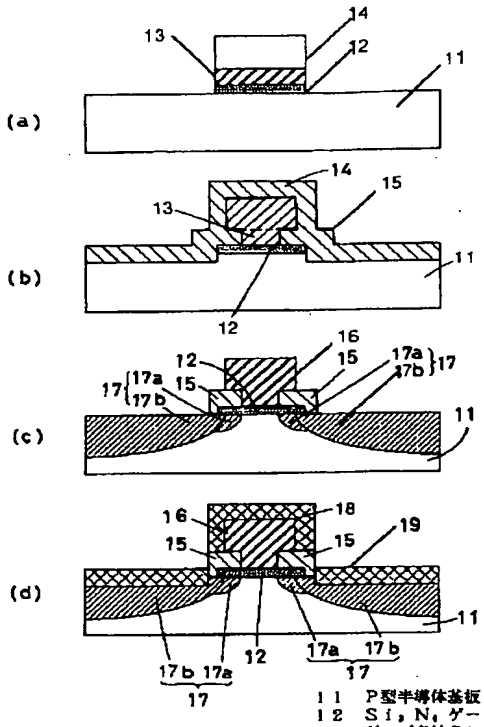
DRAWINGS

[Drawing 1]



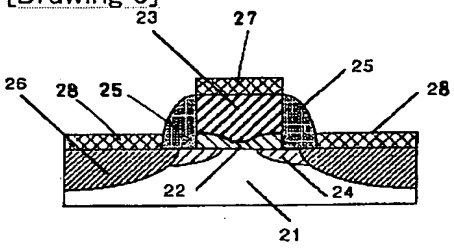
1 P型半導体基板
2 Si3N4ゲート絶縁膜
3 側壁酸化膜
4 ゲート電極
5 N型高濃度拡散層
5 a 浅いN型高濃度拡散層
5 b 深いN型高濃度拡散層
6 金属シリサイド膜
7 金属シリサイド膜

[Drawing 2]



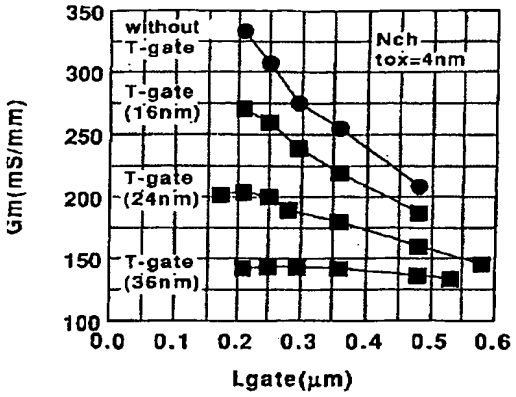
11 P型半導体基板
12 Si_3N_4 ゲート絶縁膜
13 ドープ多結晶シリコン
14 ノンドープ多結晶シリコン
15 側壁酸化膜
16 ゲート電極
17 N型高濃度拡散層
17a 浅いN型高濃度拡散層
17b 深いN型高濃度拡散層
18 金属シリサイド膜
19 金属シリサイド膜

[Drawing 3]



21 P型半導体基板
22 ゲート酸化膜
23 ゲート電極
24 浅いN型高濃度拡散層
25 SiO_2 サイドウォール
26 深いN型高濃度拡散層
27 金属シリサイド膜
28 金属シリサイド膜

[Drawing 4]



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	21/28	３０１			21/28	３０１Ｄ	
	21/336				29/78	３０１Ｌ	
						３０１Ｓ	

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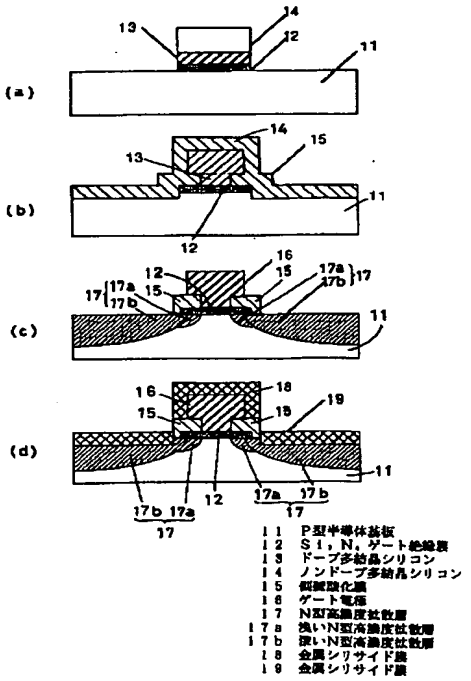
(54)【発明の名称】　ＭＯＳ型半導体装置およびその製造方法

(57)【要約】

・【課題】　駆動力を増大させつつゲート・ドレイン間容量を低減させるとともにゲート抵抗を低減させる。

・【解決手段】　Ｐ型Ｓｉ基板１１上にＳｉ$_3$Ｎ$_4$ゲート絶縁膜１２を介し、ゲート電極形成用の導電体層として、ドープ多結晶シリコン１３とノンドープ多結晶シリコン１４を堆積し、パターニングした後、Ｐ型Ｓｉ基板１１とドープ多結晶シリコン１３とノンドープ多結晶シリコン１４を酸化すると、ドープ多結晶シリコン１３が他の部分に比べて酸化速度が大きいことから、下部に一対の側壁酸化膜１５を有する理想的なＴ型構造のゲート電極１６ができる。また、Ｐ型Ｓｉ基板にイオン注入によって形成されるＮ型高濃度拡散層１７の浅い接合深さを有する部分のＰ型Ｓｉ基板１１の表面での接合部が一対の側壁酸化膜１５の対向端部と一致している。また、ゲート電極１６の上部に金属シリサイド層１８を設けるだけでなく側部にも金属シリサイド層１９を形成する。



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·【特許請求の範囲】
·【請求項１】　第１導電型の半導体基板と、
前記半導体基板の一主面に選択的に形成したゲート絶縁膜と、
前記ゲート絶縁膜上に設けられたゲート電極と、
前記ゲート電極の両端部と前記ゲート絶縁膜の間に形成されて前記ゲート電極の両端位置より外方まで延びた一対の側壁酸化膜と、
前記半導体基板の前記ゲート絶縁膜を挟む領域に形成され前記一対の側壁酸化膜の下で浅い接合深さを有するとともに前記半導体基板表面における接合位置が前記一対の側壁酸化膜の対向端部と一致しソース／ドレインとなる一対の第２導電型の高濃度拡散層と、
前記ゲート電極の上部および側部にわたって形成した第1の金属シリサイド膜とを備えたＭＯＳ型半導体装置。
·【請求項２】　ゲート絶縁膜が窒化膜である請求項１記載のＭＯＳ型半導体装置。
·【請求項３】　一対の第２導電型の高濃度拡散層の表層部に第２の金属シリサイド膜を形成したことを特徴とする請求項１または請求項２記載のＭＯＳ型半導体装置。
·【請求項４】　第１導電型の半導体基板の一主面にゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上にイオンがドーピングされた第１の導電性膜とイオンがドーピングされていない第２の導電性膜を順に堆積する工程と、
前記第２の導電性膜上のゲート電極になる所定の位置にフォトレジストをパターニングする工程と、
前記フォトレジストをマスクとして前記ゲート絶縁膜，前記第１の導電性膜および前記第２の導電性膜からなる多層膜を垂直方向に強い異方性エッチングにより前記半導体基板の一主面が露出するまで選択的にエッチングする工程と、
前記フォトレジストを除去する工程と、
酸化工程により前記第１の導電性膜の側部に成長する酸化膜が前記第２の導電性膜の側部および上部と前記半導体基板に成長する酸化膜より厚くなるような一対の側壁酸化膜を形成する工程と、
等方性のエッチングにより前記第２の導電性膜の側部および上部と前記半導体基板に成長した酸化膜を除去し、前記第１の導電性膜の側部に成長した酸化膜を前記第２の導電性膜の側部より突出した状態に残置させる工程と、
イオン注入法により前記一対の側壁酸化膜の下で浅い接合深さを有するとともに前記半導体基板表面における接合位置が前記一対の側壁酸化膜の対向端部と一致しソース／ドレインとなる一対の第２導電型の高濃度拡散層を前記半導体基板の前記ゲート絶縁膜を挟む領域に形成する工程と、
前記半導体基板および前記ゲート電極上に金属膜を堆積する工程と、

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前記ゲート電極の上部および側部と前記一対の第２導電型の高濃度拡散層の表層部に位置する前記金属膜をシリサイド化する工程と、
シリサイド化されなかった前記金属膜を除去する工程とを含むＭＯＳ型半導体装置の製造方法。
·【請求項５】　ゲート絶縁膜が窒化膜である請求項４記載のＭＯＳ型半導体装置の製造方法。
·【請求項６】　第１および第２の導電性膜が多結晶シリコン膜である請求項４または請求項５記載の記載のＭＯＳ型半導体装置の製造方法。
·【発明の詳細な説明】
·【０００１】
·【発明の属する技術分野】この発明は、集積回路の超高集積化を実現することができ、高速動作が可能で、かつ低消費電力のＭＯＳ型半導体装置およびその製造方法に関するものである。
·【０００２】
·【従来の技術】超集積回路装置いわゆるＶＬＳＩにおいて、ＭＯＳ型半導体装置は、超高集積化、高速動作および低消費電力化の要請からデバイスの微細化が行われている。このデバイスの微細化に伴い、寄生効果すなわち寄生容量、寄生抵抗の増大により、もはやスケーリングのトレンドに従った回路特性を維持できなくなりつつある。具体的には以下の２つの大きな問題点がある。
·【０００３】１）回路特性に大きな影響を及ぼすゲート・ドレイン間容量のうち、微細化に伴いゲート・ドレインオーバラップ容量（ゲート電極とドレイン領域が対向している部分に生じる容量）は減少するが、フリンジ容量（ゲート電極の側壁とドレイン領域の間に生じる容量）はスケーリングされずに一定、むしろ酸化膜が薄くなるために増加する。したがって、ゲート・ドレイン間容量の全体に占めるフリンジ容量の割合は増加し、スケーリングに見合った回路特性は期待できない。
·【０００４】２）ゲート長の減少による単位ゲート幅のゲート抵抗の増加により、同じゲート幅で比較すると、微細化に伴ってゲート電極のＲＣ遅延効果の全体の遅延時間に占める割合は増大する。これらの２つの問題点を解決する手段としては以下のような例がある。１）のゲート・ドレイン間容量を低減する構造としてはＴ形ゲート構造があり、また、２）のゲート抵抗を低減する構造としてはサリサイドプロセスがある。その代表的な文献としては、１）では例えばI.E.E.E 1991 I.E.D.M. Technical Digest pp541-544に、２）では例えばIEEE Trans. on ED, ED-29, 1982, pp531-535に紹介されている。
·【０００５】以上のＴ型ゲート構造およびサリサイドプロセスを用いたＭＯＳ型半導体装置（ＭＯＳＦＥＴ）の例を図３に示す。図３において、２１はＰ型不純物を添加したＳｉ基板からなるＰ型半導体基板、２２はＰ型半導体基板２１の主面に選択的に形成したゲート酸化膜、２３はゲート酸化膜２２上に形成したＴ形のゲート電

極、２４は浅いＮ型高濃度拡散層（２×１０^{19}ｃｍ$^{-3}$程度）、２５はＳｉO_2サイドウォール、２６は深いＮ型高濃度拡散層（２×１０^{20}ｃｍ$^{-3}$程度）、２７はサリサイドプロセスによりゲート電極の上部に形成した金属シリサイド膜、２８はサリサイドプロセスによりＮ型高濃度拡散層の表層部に形成した金属シリサイド膜である。

・【０００６】

・【発明が解決しようとする課題】しかしながら、上記のようなＴ型ゲート構造およびサリサイドプロセスを採用した構造は、ディープサブミクロン領域以下のＭＯＳ型半導体装置として十分ではない。その理由は、従来のＴ型ゲート構造ではゲート長が小さくなっても、構造上駆動力があまり増加しないためである。

・【０００７】図４は従来例のＮチャネルＭＯＳＦＥＴのトランスコンダクタンスとゲート長の関係を示す図であり、横軸がゲート長Ｌgate（μｍ）を示し、縦軸が単位ゲート幅あたりのトランスコンダクタンスＧｍ（ｍＳ／ｍｍ）を示している。なお、トランスコンダクタンスＧｍはＮチャネルＭＯＳＦＥＴのドレイン電流をＩｄｓとし、ゲート電圧をＶｇｓとしたときに、∂Ｉｄｓ／∂Ｖｇｓで表される。

・【０００８】図４において、一番上の曲線が通常の構造のＮチャネルＭＯＳＦＥＴの特性であり、下の３本の曲線がＴ型ゲート構造のＮチャネルＭＯＳＦＥＴの特性で各々再酸化膜厚が１６ｎｍ，２４ｎｍ，３６ｎｍに対応している。このＭＯＳ型ＦＥＴは、ゲート酸化膜厚t_{OX}が４ｎｍであり、シングルドレイン構造である。図４より、通常の構造では、ゲート長が小さくなるとトランスコンダクタンスが増加するのに対して、Ｔ型ゲート構造では、ゲート長が小さくなってもトランスコンダクタンスがあまり増加せず、駆動力が増加しない。

・【０００９】その理由は以下に説明する通りである。つまり、ゲート端に細長いバーズビークができ、その先端位置を正確に制御するのはきわめて困難であり、したがって図３のＰ型半導体基板２１の表面におけるＰ型半導体基板２１と浅いＮ型高濃度拡散領域２４の境界、つまりＰ型半導体基板２１と浅いＮ型高濃度拡散領域２４の接合位置をＴ型のゲート電極２３の脚部の端部にちょうど合わせるのが困難である。接合位置の間隔を狭く設定すると、場合によっては、ソースおよびドレインの両方の浅いＮ型高濃度拡散領域２４がＰ型半導体基板２１の表面でつながってしまい、ＭＯＳ型半導体装置のチャネルがなくなるので、接合位置がＴ型のゲート電極２３の脚部の直下より外寄りになるように、浅いＮ型高濃度拡散領域２４を形成せざるを得ない。

・【００１０】ところが、上述の接合位置が厚い酸化膜の領域（Ｔ型のゲート電極２３の脚部より外側の領域）にかかると、Ｐ型半導体基板２１の表面におけるＴ型のゲート電極２３の脚部の端から接合位置までの間の領域は、ゲート電極２３との間のゲート酸化膜２２の膜厚が

厚くなっているので電界が加わりにくく、しかも、Ｎ型にドープされておらずＰ型のままであるので、ゲート電極２３にゲート電圧を加えることにより、Ｔ型のゲート電極２３の脚部の直下にチャネル部を形成したとしても、チャネル部から浅いＮ型高濃度拡散層２４のまでのＰ型領域が非常に大きな寄生抵抗になり、たとえチャネル部の抵抗が小さくても、全体のトランスコンダクタンスはその寄生抵抗で律則されてしまい、ゲート長が短くなるにもかかわらず駆動力が増加しない。また、中心部の酸化膜厚も再酸化によるバーズビークの成長によって厚くなるため、実効的なゲート酸化膜厚が増大し、チャネル部の抵抗が増加する。この現象はゲート長が小さくなるほど顕著になる。この点でも駆動力の増加を制限している。

・【００１１】また、ゲート幅が１０μｍで、ゲート酸化膜厚が４ｎｍのＭＯＳＦＥＴでは、シート抵抗が１０オーム／□程度であると仮定すると、そのゲート電極のＲＣ遅延は９ｐｓ程度になる。このＲＣ遅延は、シート抵抗が一定ならば、ゲート長によらず一定である。例えばゲート長が０．１５μｍのＣＭＯＳプロセスにおいては、そのゲート遅延は３０ｐｓ程度と予測され、ゲート電極のＲＣ遅延は全体の約１／３と非常に大きなものとなる。

・【００１２】この発明の目的は、ディープサブミクロン領域以下において、駆動力を増加させつつゲート・ドレイン間容量を低減することができるとともに、ゲート抵抗を十分に低減することができるＭＯＳ型半導体装置およびその製造方法を提供することである。

・【００１３】

・【課題を解決するための手段】請求項１記載のＭＯＳ型半導体装置は、第１導電型の半導体基板の一主面にゲート絶縁膜を選択的に形成し、ゲート絶縁膜上にゲート電極を設け、ゲート電極の両端部とゲート絶縁膜の間にゲート電極の両端位置より外方まで延びた一対の側壁酸化膜を形成し、半導体基板のゲート絶縁膜を挟む領域に一対の側壁酸化膜の下で浅い接合深さを有するとともに半導体基板表面における接合位置が一対の側壁酸化膜の対向端部と一致しソース／ドレインとなる一対の第２導電型の高濃度拡散層を形成し、ゲート電極の上部および側部にわたって第１の金属シリサイド膜を形成している。

・【００１４】このＭＯＳ型半導体装置によると、ゲート電極の両端部とゲート絶縁膜の間にゲート電極の両端位置より外方まで延びた一対の側壁酸化膜が形成され、ゲート電極がＴ型ゲート構造となり、ゲート電極の側部とドレイン／ソースである一対の第２導電型の高濃度拡散層との間の距離が増加し、したがってゲート・ドレイン間容量が低減される。また、一対の第２導電型の高濃度拡散層の半導体基板表面における接合位置が一対の側壁酸化膜の対向端部と一致するので、ゲート絶縁膜下のチャネル部となる半導体基板の領域の全体にゲート電圧が

有効に加えられ、一対の側壁酸化膜下に高抵抗の部分が残ることはないので、Ｔ型ゲート構造に伴いゲート長が短くなった分だけ駆動力が増加することになる。また、ゲート電極の上部だけでなく側部にも第１の金属シリサイド膜が形成されるので、ゲート抵抗が十分に低減される。また、第２の高濃度拡散層が一対の側壁酸化膜の下で浅い接合深さを有しているので、ショートチャネル効果に非常に強いデバイスとなる。

・【００１５】請求項２記載のＭＯＳ型半導体装置は、請求項１記載のＭＯＳ型半導体装置において、ゲート絶縁膜を窒化膜としている。このＭＯＳ型半導体装置によると、ゲート絶縁膜からその上のゲート電極への酸素の供給が遮断され、ゲート絶縁膜上に一対の側壁酸化膜を形成する際に酸素はゲート電極の側壁から供給されるのみとなり、ゲート電極の中心部へは酸素が供給されないので、酸化膜はゲート電極の側壁からゲート電極の内部に向かってゲート絶縁膜と略平行に進行することになり、一対の側壁酸化膜がバーズビーク状になるのが抑えられて略四角形に近い状態となり、ゲート電極が理想的なＴ型に近い状態となる。したがって、Ｔ型の脚部を細くせずにＴ型の脚部を長くすることが容易となり、ゲート・ドレイン間容量が一層低減される。

・【００１６】請求項３記載のＭＯＳ型半導体装置は、請求項１または請求項２記載のＭＯＳ型半導体装置において、一対の第２導電型の高濃度拡散層の表層部に第２の金属シリサイド膜を形成している。このＭＯＳ型半導体装置によると、ソース／ドレインの抵抗も減少することになる。請求項４記載のＭＯＳ型半導体装置の製造方法は、第１導電型の半導体基板の一主面にゲート絶縁膜を形成し、このゲート絶縁膜上にイオンがドーピングされた第１の導電性膜とイオンがドーピングされていない第２の導電性膜を順に堆積し、ついで第２の導電性膜上のゲート電極になる所定の位置にフォトレジストをパターニングし、フォトレジストをマスクとしてゲート絶縁膜，第１の導電性膜および第２の導電性膜からなる多層膜を垂直方向に強い異方性エッチングにより半導体基板の一主面が露出するまで選択的にエッチングする。その後、フォトレジストを除去し、酸化工程により第１の導電性膜の側部に成長する酸化膜が第２の導電性膜の側部および上部と半導体基板に成長する酸化膜より厚くなるような一対の側壁酸化膜を形成し、ついで等方性のエッチングにより第２の導電性膜の側部および上部と半導体基板に成長した酸化膜を除去し、第１の導電性膜の側部に成長した酸化膜を第２の導電性膜の側部より突出した状態に残置させる。つぎに、イオン注入法により一対の側壁酸化膜の下で浅い接合深さを有するとともに半導体基板表面における接合位置が前記一対の側壁酸化膜の対向端部と一致しソース／ドレインとなる一対の第２導電型の高濃度拡散層を半導体基板のゲート絶縁膜を挟む領域に形成し、半導体基板およびゲート電極上に金属膜を

堆積し、ついでゲート電極の上部および側部と一対の第２導電型の高濃度拡散層の表層部に位置する金属膜をシリサイド化し、その後シリサイド化されなかった金属膜を除去する。

・【００１７】このＭＯＳ型半導体装置の製造方法によると、ゲート電極がイオンがドーピングされた第１の導電性膜（例えばドープ多結晶シリコンからなる）とイオンがドーピングされていない第２の導電性膜（例えばノンドープ多結晶シリコンからなる）の２層構造になっており、酸化工程では第１の導電性膜の酸化レートが第２の導電性膜の酸化レートより大きいために、ゲート電極の形状がＴ型になる。したがって、ゲート・ドレイン間容量が小さくなる。

・【００１８】また、半導体基板表面における接合位置が一対の側壁酸化膜の対向端部と一致させているので、ゲート絶縁膜下のチャネル部となる半導体基板の領域の全体にゲート電圧を有効に加えることができ、一対の側壁酸化膜下に高抵抗の部分が残ることはないので、Ｔ型ゲート構造に伴いゲート長が短くなった分だけ駆動力が増加することはになる。なお、駆動力を増加させることが可能であるのは、酸化レートの違いを利用して一対の側壁酸化膜を形成しているので、その長さを精度よく制御することができ、したがって、イオン注入により形成する高濃度拡散層の接合位置を一対の側壁酸化膜の対向端部に容易に合わせることができるからである。

・【００１９】また、一対の側壁酸化膜により、ゲート電極上のシリサイド層とソース／ドレインのシリサイド層とが絶縁されるために、ゲート電極の上部だけでなく側部もシリサイド化でき、ゲート抵抗が十分に低減される。また、一対の側壁酸化膜により１回の注入工程で接合深さが浅い高濃度拡散層と接合深さが深い高濃度拡散層、すなわちエクステンションソース／ドレインが形成される。

・【００２０】請求項５記載のＭＯＳ型半導体装置の製造方法は、請求項４記載のＭＯＳ型半導体装置の製造方法において、ゲート絶縁膜を窒化膜としている。このＭＯＳ型半導体装置によると、ゲート絶縁膜からその上のゲート電極への酸素の供給が遮断され、ゲート絶縁膜上に一対の側壁酸化膜を形成する際に酸素はゲート電極の側壁から供給されるのみとなり、ゲート電極の中心部には酸素は供給されない。したがって、酸化膜はゲート電極の側壁からゲート電極の内部に向かってゲート絶縁膜と略平行に進行することになり、一対の側壁酸化膜がバーズビーク状になるのが抑えられて略四角形に近い状態となり、ゲート電極が理想的なＴ型に近い状態になる。したがって、Ｔ型の脚部を細くせずにＴ型の脚部を長くすることが容易となり、ゲート・ドレイン間容量が一層低減される。

・【００２１】請求項６記載のＭＯＳ型半導体装置の製造方法は、請求項４または請求項５記載のＭＯＳ型半導体

装置の製造方法において、第１および第２の導電性膜を多結晶シリコン膜としている。

・【００２２】

・【発明の実施の形態】以下、この発明のＭＯＳ型半導体装置およびその製造方法の実施の形態について、図面を参照しながら説明する。

・〔ＭＯＳ型半導体装置の実施の形態〕図１はこの発明のＭＯＳ型半導体装置の実施の形態における断面図である。図１において、１はＰ型不純物を導入したＳｉ基板からなるＰ型半導体基板である。２はＰ型半導体基板１の一主面上に選択的に形成したSi_3N_4膜からなるゲート絶縁膜である。４はゲート絶縁膜２上に設けられたＴ型構造のゲート電極であり、その両端部はゲート絶縁膜２の端部より内方に後退している。３はゲート電極４の端部とゲート絶縁膜２の間に形成された一対の側壁酸化膜であり、その端部はゲート電極４の端部を越え、さらにゲート絶縁膜２の端部を越えて外方まで延びている。５はＰ型半導体基板１のゲート絶縁膜２を挟む領域に形成され一対の側壁酸化膜３の下で浅い接合深さを有するとともにＰ型半導体基板１の表面における接合位置が一対の側壁酸化膜３の対向端部と一致しソース／ドレインとなる一対の第２導電型の高濃度拡散層である。５ａは浅いＮ型高濃度拡散層、５ｂは深いＮ型拡散層である。６はＴ型構造のゲート電極４の上部および側部（脚部の側部を除く）にわたって形成した金属シリサイド膜であり、７は一対の第２導電型の高濃度拡散層５の表層部に形成した金属シリサイド膜であり、これはサリサイドプロセスにより形成され、一対の側壁酸化膜３で絶縁分離されている。

・【００２３】図１のＭＯＳ型半導体装置の構造で特徴的なことは、ゲート電極４の端部に略長方形の形状をした一対の側壁酸化膜３があるために、理想的なＴ型構造のゲート電極４となっており、この一対の側壁酸化膜３の対向端部に高濃度拡散層５の接合位置を合わせることと、ゲート電極４の上部だけでなく側部にも金属シリサイド膜６を形成していることと、一対の側壁酸化膜３下の高濃度拡散層５の接合深さが浅いことである。

・【００２４】なお、上記実施の形態では、ゲート絶縁膜２はシリコン窒化膜で構成していたが、シリコン酸化膜で構成してもよい。この実施の形態によると、ゲート電極４の両端部とゲート絶縁膜２の間にゲート電極４の両端位置より外方まで延びた一対の側壁酸化膜３を形成したので、Ｔ型ゲート構造となり、ゲート電極４の側部とドレインとの間の距離を稼ぐことができ、したがってゲート・ドレイン間容量を低減することができる。また、一対の第２導電型の高濃度拡散層５のＰ型半導体基板１の表面における接合位置を一対の側壁酸化膜３の対向端部と一致させたので、ゲート絶縁膜２下のチャネル部となるＰ型半導体基板１の領域の全体にゲート電圧を有効に加えることができ、一対の側壁酸化膜３下にゲート電圧が有効に加えられず高抵抗の部分が残ることはないので、Ｔ型ゲート構造に伴いゲート長が短くなった分だけ駆動力を増大させることができる。また、ゲート電極４の上部だけでなく側部にも第１の金属シリサイド膜６を形成しているので、ゲート抵抗を十分に低減することができる。また、第２の高濃度拡散層５が一対の側壁酸化膜３の下で浅い接合深さを有しているので、ショートチャネル効果に非常に強いデバイスとなる。

・【００２５】また、ゲート絶縁膜２からその上のゲート電極４への酸素の供給が遮断され、ゲート絶縁膜２上に一対の側壁酸化膜３を形成する際に酸素はゲート電極４の側壁から供給されるのみとなり、ゲート電極４の中心部へは酸素が供給されないので、酸化膜はゲート電極４の側壁からゲート電極４の内部に向かってゲート絶縁膜２と略平行に進行することになり、一対の側壁酸化膜３がバーズビーク状になるのが抑えられて略四角形に近い状態となり、ゲート電極４を理想的なＴ型に近づけることができる。したがって、Ｔ型の脚部を細くせずにＴ型の脚部を長くすることが容易となり、ゲート・ドレイン間容量を一層低減することが可能となる。また、一対の第２導電型の高濃度拡散層５の表層部に金属シリサイド膜７を形成しているので、ソース／ドレインの抵抗も減少させることができる。

・【００２６】〔ＭＯＳ型半導体装置の製造方法の実施の形態〕図２（ａ）～（ｄ）はこの発明のＭＯＳ型半導体装置の製造方法の実施の形態における工程断面図である。以下、図２を参照しながら、ＭＯＳ型半導体装置の製造方法について説明する。まず図２（ａ）に示すように、最初にＰ型Ｓｉ基板からなるＰ型半導体基板１１上にSi_3N_4ゲート絶縁膜１２を８ｎｍ程度に形成する。なお、Ｐ型半導体基板１１上とSi_3N_4ゲート絶縁膜１２には各々１～２ｎｍ程度の自然酸化膜が形成されてもよい。その場合にはSi_3N_4ゲート絶縁膜１２は４ｎｍ程度に形成し、酸化膜換算で４～５ｎｍ程度になるように設定する。なお、この場合の工程の順序としては、Ｐ型半導体基板１１上に１～２ｎｍ程度の自然酸化膜が形成された後、Si_3N_4ゲート絶縁膜１２を堆積し、さらにその後Si_3N_4ゲート絶縁膜１２上に１～２ｎｍ程度の自然酸化膜が形成されることになる。

・【００２７】つぎに、Si_3N_4ゲート絶縁膜１２上に、ドープ多結晶シリコン膜１３およびアンドープ多結晶シリコン膜１４を各々膜厚６０ｎｍ、１４０ｎｍ程度に順に堆積する。このときドープ多結晶シリコン膜１３はＮ型で、$2\times10^{20}cm^{-3}$程度にドーピングされている。さらに、アンドープ多結晶シリコン膜１４上にフォトレジスト（図示せず）を堆積し、その後アンドープ多結晶シリコン膜１４上のゲート電極１６（図２（ｃ），・（ｄ）参照）になる所定の位置にフォトレジストを残すようにパターニングする。そして、フォトレジストをマスクとして垂直方向に強い異方性エッチングを行うこと

により、選択的にゲート電極１６となる部分を残す。最後に、フォトレジストを除去する。

·【００２８】つぎに、図２（ｂ）に示すように、ウエット酸素雰囲気（H_2O+O_2雰囲気）中で８５０℃１５分の熱処理を行う。これによりアンドープ多結晶シリコン膜１４上の上部および側部にゲート電極１６の端部から外側と内側に各々１０ｎｍ、合計２０ｎｍ、Ｐ型半導体基板１１上に２０ｎｍ、またドープ多結晶シリコン膜１３の側部にゲート端から外側と内側に各々４０ｎｍ、合計８０ｎｍの側壁酸化膜１５を形成する。なお、上記の熱処理によって、不純物が拡散したドープ多結晶シリコン１３とノンドープ多結晶１４は一体のものとなる。

·【００２９】つぎに、図２（ｃ）に示すように、NH_4F：ＨＦ＝２０：１、２０℃、２０秒の条件のウエットエッチング（等方性エッチング）により、アンドープ多結晶シリコン膜１４上の上部および側部とＰ型半導体基板１１上に形成された側壁酸化膜１５を除去する。このとき、ドープ多結晶シリコン膜１３の側部の側壁酸化膜はゲート電極１６の端部から外側と内側に各々３０ｎｍ、また高さが４０ｎｍとなる。上記工程は等方性のドライエッチングでも可能である。

·【００３０】つぎに、Ｎ型の不純物、注入エネルギー２０ｋｅＶ、注入ドーズ量4×10^{15}程度の条件で、例えばＡｓイオンのイオン注入を行うことで、Ｎ型のゲート電極１６およびＰ型半導体基板上１１にソース／ドレインとなるＮ型高濃度拡散層１７を形成する。さらに、ラシプアニール（ＲＴＡ；ラピッドサーマルアニール）を１０００℃、１０ｓｅｃの条件で行うことで、ソース／ドレインおよびゲート電極１６の活性化を同時に行う。このとき、Ｎ型高濃度拡散層１７の一対の側壁酸化膜１５下の浅いＮチャネル高濃度拡散層１７ａの接合深さは５０ｎｍ程度、それ以外のソース／ドレインの深いＮ型高濃度拡散層１７の接合深さは１００ｎｍ程度になる。また、ソース／ドレインのオーバラップ長は３０ｎｍ程度になり、ソース／ドレインとなるＮ型高濃度拡散層１７の接合位置と一対の側壁酸化膜１５の対向端部の位置が一致する。なお、このようにＮ型高濃度拡散層１７の接合位置と一対の側壁酸化膜１５の対向端部の位置をほぼ一致させるためには、ランプアニールの条件およびイオン注入の条件を適正に設定する必要がある。

·【００３１】つぎに、図２（ｄ）に示すように、金属膜としてＣｏを１０ｎｍ程度、ＴｉＮを２０ｎｍ程度順に堆積させる（Ｃｏの酸化防止のために２層構造としている）。第１の熱処理を４５０℃、３０分行うことでゲート電極１６およびＰ型半導体基板上１１のソース／ドレインとなる高濃度拡散層１７をシリサイド化する（サリサイドプロセス）。さらに、シリサイド化されなかったＣｏ／ＴｉＮ層を$NH_4OH+H_2O_2+H_2O$（６５℃、９０秒）および$HCl+H_2O_2$·（室温、３分）の条件でエッチングすることで金属シリサイド膜１８，１９を形成する。さらに、金属シリサイド膜１８，１９の低抵抗化を図るため、第２の熱処理を７５０℃、３０秒のＲＴＡで行う。

·【００３２】以上のように構成されたＭＯＳ型半導体装置の製造方法の実施の形態では、ゲート電極１６がドープ多結晶シリコン膜１３とアンドープ多結晶シリコン膜１４の２層構造になっており、酸化工程ではドープ多結晶シリコン膜１３の酸化レートが大きいために、ゲート電極１６の形状をＴ型にすることができる。この際、酸化レートの違いを利用して一対の側壁酸化膜１５を形成しているので、その長さを精度よく制御することができ、したがって、イオン注入により形成する高濃度拡散層１７の接合位置を一対の側壁酸化膜１５の対向端部に容易に合わせることができ、したがって駆動力を容易に増加させることができる。また、ゲート絶縁膜１２として窒化シリコン膜を用いているために、ゲート電極１６の中心部には酸素が供給されず、ゲート電極１６の端部にバーズビークが形成されないために、理想的なＴ型構造のゲート電極１６を作ることができる。また、一対の側壁酸化膜１５によりゲート電極４上の金属シリサイド膜１８とソース／ドレインとなる高濃度拡散層１７上の金属シリサイド膜１９とを絶縁できるために、ゲート電極１６の上部だけでなく側部もシリサイド化できる。また、一対の側壁酸化膜１５の存在により１回の注入工程で接合深さが浅い高濃度拡散層１７ａと接合深さが深い高濃度拡散層１７ｂ、すなわちエクステンションソース／ドレインを形成できる。

·【００３３】

·【発明の効果】請求項１記載のＭＯＳ型半導体装置によれば、ゲート電極の両端部とゲート絶縁膜の間にゲート電極の両端位置より外方まで延びた一対の側壁酸化膜を形成したので、Ｔ型ゲート構造となり、ゲート電極の側部とドレインとの間の距離を稼ぐことができ、したがってゲート・ドレイン間容量を低減することができる。また、一対の第２導電型の高濃度拡散層の半導体基板表面における接合位置を一対の側壁酸化膜の対向端部と一致させたので、ゲート絶縁膜下のチャネル部となる半導体基板の領域の全体にゲート電圧を有効に加えることができ、一対の側壁酸化膜下に高抵抗の部分が残ることはないので、Ｔ型ゲート構造に伴いゲート長が短くなった分だけ駆動力を増大させることができる。また、ゲート電極の上部だけでなく側部にも第１の金属シリサイド膜を形成しているので、ゲート抵抗を十分に低減することができる。また、第２の高濃度拡散層が一対の側壁酸化膜の下で浅い接合深さを有しているので、ショートチャネル効果に非常に強いデバイスとなる。

·【００３４】請求項２記載のＭＯＳ型半導体装置によれば、ゲート絶縁膜からその上のゲート電極への酸素の供給が遮断され、ゲート絶縁膜上に一対の側壁酸化膜を形成する際に酸素はゲート電極の側壁から供給されるのみ

となり、ゲート電極の中心部へは酸素が供給されないので、酸化膜はゲート電極の側壁からゲート電極の内部に向かってゲート絶縁膜と略平行に進行することになり、一対の側壁酸化膜がバーズビーク状になるのが抑えられて略四角形に近い状態となり、ゲート電極を理想的なＴ型に近づけることができる。したがって、Ｔ型の脚部を細くせずにＴ型の脚部を長くすることが容易となり、ゲート・ドレイン間容量を一層低減することが可能となる。

・【００３５】請求項３記載のＭＯＳ型半導体装置によれば、ソース／ドレインの抵抗も減少させることができる。請求項４記載のＭＯＳ型半導体装置の製造方法によれば、ゲート電極がイオンがドーピングされた第１の導電性膜とイオンがドーピングされていない第２の導電性膜の２層構造になっており、酸化工程では第１の導電性膜の酸化レートが第２の導電性膜であるノンドープ多結晶シリコンの酸化レートより大きいために、ゲート電極の形状をＴ型にすることができる。したがって、ゲート・ドレイン間容量を小さくすることができる。

・【００３６】また、半導体基板表面における接合位置を一対の側壁酸化膜の対向端部と一致させているので、ゲート絶縁膜下のチャネル部となる半導体基板の領域の全体にゲート電圧を有効に加えることができ、一対の側壁酸化膜下にゲート電圧が有効に加えられず高抵抗の部分が残ることはないので、Ｔ型ゲート構造に伴いゲート長が短くなった分だけ駆動力を増大させることができる。なお、駆動力を容易に増加させることができるのは、酸化レートの違いを利用して一対の側壁酸化膜を形成しているので、その長さを精度よく制御することができ、したがって、イオン注入により形成する高濃度拡散層の接合位置を一対の側壁酸化膜の対向端部に容易に合わせることができるからである。

・【００３７】また、一対の側壁酸化膜により、ゲート電極上のシリサイド層とソース／ドレインのシリサイド層とを絶縁できるためにゲート電極の上部だけでなく側部もシリサイド化でき、ゲート抵抗を十分に低減することができる。また、一対の側壁酸化膜により１回の注入工程で接合深さが浅い高濃度拡散層と接合深さが深い高濃度拡散層、すなわちエクステンションソース／ドレインを形成できる。

・【００３８】請求項５記載のＭＯＳ型半導体装置の製造方法によれば、ゲート絶縁膜からその上のゲート電極への酸素の供給が遮断され、ゲート絶縁膜上に一対の側壁酸化膜を形成する際に酸素はゲート電極の側壁から供給されるのみとなり、ゲート電極の中心部には酸素は供給されないので、酸化膜はゲート電極の側壁からゲート電

極の内部に向かってゲート絶縁膜と略平行に進行することになり、一対の側壁酸化膜がバーズビーク状になるのが抑えられて略四角形に近い状態となり、ゲート電極を理想的なＴ型に近づけることができる。したがって、Ｔ型の脚部を細くせずにＴ型の脚部を長くすることが容易となり、ゲート・ドレイン間容量を一層低減することが可能となる。

・【図面の簡単な説明】

・【図１】この発明のＭＯＳ型半導体装置の実施の形態を示す構造断面図である。

・【図２】この発明のＭＯＳ型半導体装置の製造方法の実施の形態を示す構造断面図である。

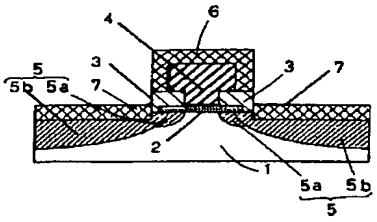
・【図３】従来例のＭＯＳ型半導体装置を示す構造断面図である。

・【図４】従来例のＭＯＳ型半導体装置のトランスコンダクタンスとゲート長の関係を示す図である。

・【符号の説明】

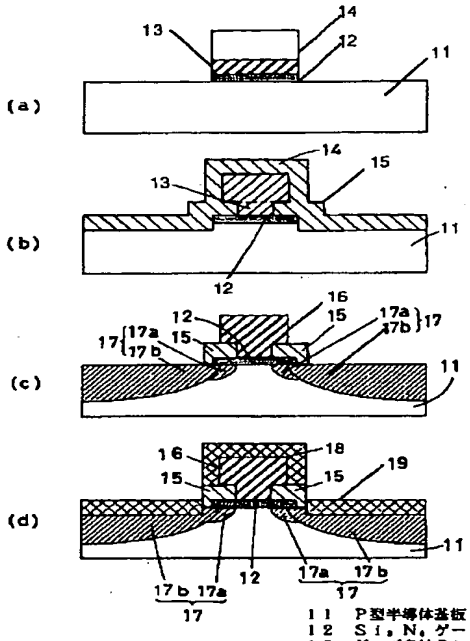
・１　Ｐ型半導体基板
２　Si_3N_4 ゲート絶縁膜
３　側壁酸化膜
４　ゲート電極
５　Ｎ型高濃度拡散層
５ａ　浅いＮ型高濃度拡散層
５ｂ　深いＮ型高濃度拡散層
６　金属シリサイド膜
７　金属シリサイド膜
・１１　Ｐ型半導体基板
・１２　Si_3N_4 ゲート絶縁膜
・１３　ドープ多結晶シリコン
・１４　ノンドープ多結晶シリコン
・１５　側壁酸化膜
・１６　ゲート電極
・１７　Ｎ型高濃度拡散層
・１７ａ　浅いＮ型高濃度拡散層
・１７ｂ　深いＮ型高濃度拡散層
・１８　金属シリサイド膜
・１９　金属シリサイド膜
２１　Ｐ型半導体基板
２２　ゲート酸化膜
２３　ゲート電極
２４　浅いＮ型高濃度拡散層
２５　SiO_2 サイドウォール
２６　深いＮ型高濃度拡散層
２７　金属シリサイド膜
２８　金属シリサイド膜

・【図１】



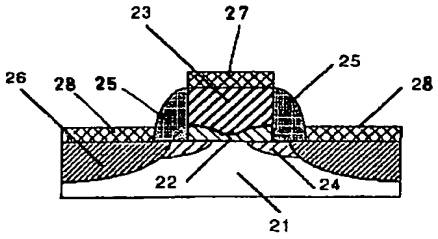
1　P型半導体基板
2　Si_3N_4 ゲート絶縁膜
3　側壁酸化膜
4　ゲート電極
5　N型高濃度拡散層
5 a　浅いN型高濃度拡散層
5 b　深いN型高濃度拡散層
6　金属シリサイド膜
7　金属シリサイド膜

・【図２】



11　P型半導体基板
12　Si_3N_4 ゲート絶縁膜
13　ドープ多結晶シリコン
14　ノンドープ多結晶シリコン
15　側壁酸化膜
16　ゲート電極
17　N型高濃度拡散層
17a　浅いN型高濃度拡散層
17b　深いN型高濃度拡散層
18　金属シリサイド膜
19　金属シリサイド膜

・【図３】



21　P型半導体基板
22　ゲート酸化膜
23　ゲート電極
24　浅いN型高濃度拡散層
25　SiO_2 サイドウォール
26　深いN型高濃度拡散層
27　金属シリサイド膜
28　金属シリサイド膜

・【図４】